REMARKS

Claims 45, 46, 50-52, 54, 56, 59, 60, 68-70, 73, 74 and 77 are pending in this application. Claims 73 and 77 have been amended.

Applicant notes that the listing of allowed claims on the Office Action Summary omits claim 69, which is indicated in the body of the Office action as having been allowed.

Claims 54, 56, 73, 74, and 77 stand rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,702,976 to Schuegraf et al., in view of U.S. Patent No. 3,755,001 to Kooi et al., and in view of U.S. Patent No. 5,841,163 Joo et al. This rejection is respectfully traversed.

Claim 73 recites a memory device having "a semiconductor substrate including a plurality of doped active regions, said semiconductor substrate having a first doping concentration," and "a field isolation region separating at least two of said active regions, said field isolation region including an isolation trench, said isolation trench further including a first area filled with a first dielectric material forming at least sidewalls of said isolation trench, and a second area filled with a second dielectric material situated within said sidewalls, said first dielectric material being different than said second dielectric material." An ion implanted region is provided "below and aligned with said second area and having an increased doping concentration in an area of said substrate between said separated active regions, said increased doping concentration being higher than said first doping concentration of said substrate." In addition, "substantially all ions from said ion implanted region which increase said doping concentration are displaced away from said active regions and are aligned by the sidewalls of said isolation trench."

The Schuegraf et al. reference relates to a DRAM having small, shallow isolation trenches. The reference to Schuegraf et al. recognizes that "field threshold voltage is influenced by a number of physical and material properties of the trench isolator such as insulator thickness, dielectric constant, substrate doping, field implant dose and substrate bias," and acknowledges that "a principal difficulty in decreasing the trench depth is the compromise in device isolation." To compensate for compromised device isolation, the Schuegraf et al. reference lines the

disclosed shallow isolation trenches with dielectric materials having a lower dielectric constant than used in the prior art. See Col. 2, lines 61-63; Figure 3D. To avoid contamination of substrate regions adjacent to trenches 22, Schuegraf further teaches "it is preferable to form a barrier layer 24 over the trenches 22 prior to dielectric refill." (Col. 5, lines 9-12; Figure 3B). In this manner, by "utilizing dielectric materials having a lower dielectric constant than used in the prior art," the shallow isolation trench of Schuegraf "maintains effective device isolation." (Col. 4, lines 37-40). Schuegraf et al. is silent, however, regarding a field isolation region having first area of dielectric material forming sidewalls of an isolation trench, and a second area filled with a second dielectric material situated within the sidewalls, the isolation region including an ion implant region "below and aligned with said second area, and having an increased doping concentration in an area of said substrate" between separated active regions. In addition, Schuegraf et al. contains no mention of an isolation region in which "substantially all ions from said ion implanted region which increase said doping concentration are displaced away from said active regions and are aligned by the sidewalls of said isolation trench."

Recognizing the deficiencies of Schuegraf et al., the Examiner relies on Kooi et al. and Joo et al. to supply missing teachings.

Kooi et al. relates to a method of fabricating semiconductor devices having selective doping and selective oxidation. Implant regions 6, 28, and 44 are formed in *unlined* trenches, are ion implanted using a projecting edge of a *mask* for alignment, and are filled with oxide *after* the implanting takes place. Consequently, Kooi et al., taken alone or in combination with Schuegraf et al., does not teach or suggest an ion implanted region provided "below and aligned with" a second area "filled with a second dielectric material situated" within the sidewalls. Further, Kooi et al. does not teach or suggest that "substantially all ions from said ion implanted region which increase said doping concentration are displaced away from said active regions and are aligned by the sidewalls of said isolation trench."

The reference to Joo et al. relates to integrated circuit structures having channel stop layers formed by employing first and second field insulation layers coupled with first and second channel stop impurity layers. See col. 3, lines 38-47 of Joo et al. For example, Joo et al. discloses that impurity ions are implanted below the first field oxide layer and are diffused by a

thermal process to form a second channel stop impurity layer. (Col. 6, lines 36-50; Figure 15.) Joo et al. discloses, however, that ion implantation is aligned using a photoresist. Thus, Joo et al., taken alone or in combination, does not teach or suggest a field isolation region having first area dielectric material forming sidewalls of an isolation trench, a second area filled with a second dielectric material situated within the sidewalls, and an ion implant region "below and aligned with said second area." In addition, Joo et al. contains no teaching of an isolation region in which "substantially all ions from said ion implanted region which increase said doping concentration are displaced away from said active regions and are aligned by the sidewalls of said isolation trench." Claim 73 and its dependent claims 54, 56, 59, 60, and 74 are submitted as patentable over the cited references to Schuegraf et al., Kooi et al., and Joo et al.

Claim 77 recites an integrated circuit having "a semiconductor substrate including a first region of a predefined conductivity type," "a field isolation region for separating said first region into at least two active regions, wherein said field isolation region includes an isolation trench, said isolation trench further including a first dielectric material forming sidewalls of said isolation trench and provided on a bottom of said isolation trench, said sidewalls having a thickness, and a second dielectric material situated within said sidewalls and provided over said first dielectric material, said first dielectric material being different than said second dielectric material. At least a portion of a memory cell is "provided in at least one of said two active regions." Also included is "a doped region formed within said first region and below said isolation trench, said doped region being of said predefined conductivity type and having a doping concentration higher than a doping concentration of said first region." Further, "additional dopants in said doped region causing said higher dopant concentration are aligned by said sidewalls and are displaced away from said separated active regions."

The reference to Schuegraf et al. discloses an integrated circuit including devices formed with small, shallow isolation trenches. Reduced device isolation due to the shallow trenches is compensated by filling the trenches with material having a lower dielectric constant than that of silicon oxide. The Schuegraf et al. reference teaches devices having isolation trenches filled with a low-constant dielectric material and a barrier layer, but does not disclose "a doped region formed within said first region, and below said isolation trench, said doped region being of said predefined conductivity type and having a doping concentration higher than a

doping concentration of said first region." Further, the reference to Schuegraf et al. does not disclose that "additional dopants in said doped region causing said higher dopant concentration are aligned by" sidewalls formed in the trench, and "are displaced away from said separated active regions."

The Examiner turns to Kooi et al. and Joo et al. to supply that which is missing from Schuegraf et al. Kooi et al. discloses ion implants formed in the bottom of unlined trenches and aligned by the projection edges of a mask. Kooi et al. does not teach or suggest that "additional dopants in said doped region causing said higher dopant concentration are aligned by" sidewalls formed in the trench. The reference to Kooi et al. also does not disclose "a doped region formed within said first region, and below said isolation trench, said doped region being of said predefined conductivity type and having a doping concentration higher than a doping concentration of said first region." The Joo et al. reference does not disclose that "additional dopants in said doped region causing said higher dopant concentration are aligned by" sidewalls formed in the trench, but rather uses a photoresist mask for alignment, and further does not teach or suggest "a doped region formed within said first region, and below said isolation trench." Schuegraf et al., Kooi et al., and Joo et al., taken alone or in combination, do not render obvious the invention recited by claim 77.

Given that not all claim limitations are taught or suggested by the cited references, the Office action fails to establish a *prima facie* case of obviousness. Applicant further notes that the proposed combination of Schuegraf et al., Kooi et al., and Joo et al. lacks the suggestion or motivation required for a proper rejection under 35 U.S.C. § 103. On the contrary, as noted specifically above, Schuegraf et al. discloses forming a barrier layer in a trench, and then filling the trench. Schuegraf et al. does not teach or suggest forming an ion implant using a trench sidewall for alignment. Kooi et al. and Joo et al. use masks for implant alignment, and so cannot provide the suggestion or motivation to form an ion implant aligned by a trench sidewall. The Examiner's unsupported "conclusion" that the claimed structures would have been obvious lacks the required motivation from the prior art for combining the cited references. Instead, the proposed combination of references appears to be an attempt at improper hindsight reconstruction of the invention using Applicant's disclosure as a guide. Applicant respectfully submits that the Office has not met its burden of proving a *prima facie* case of obviousness.

Applicant's amendment is believed to put the application in condition for allowance. Withdrawal of the rejection of claims 54, 56, 73, 74 and 77 is requested. Allowance of the application is solicited.

Dated: February 24, 2004

Respectfully submitted,

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